PRODUCT/PROCESS CHANGE NOTIFICATION

PCN APG-BAD/12/7432
Dated 10 Sep 2012

VIPower M03 / M03.5 in SOT-223: Assembly Transfer from Carsem to Fujitsu Subcontractor

Table 1. Change Implementation Schedule

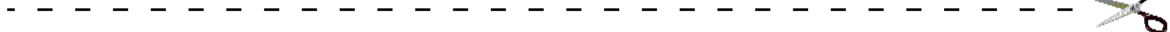
Forecasted implementation date for change	30-Nov-2012
Forecasted availability date of samples for customer	03-Sep-2012
Forecasted date for **STMicroelectronics** change Qualification Plan results availability	03-Sep-2012
Estimated date of changed product first shipment	10-Dec-2012

Table 2. Change Identification

Product Identification (Product Family/Commercial Product)	see enclosed list
Type of change	Package assembly location change
Reason for change	Logistic
Description of the change	Please be informed that VIPower M03 / M03.5 products housed in SOT-223 will be transferred from assembly Carsem to Fujitsu Subcontractor.Due to all the products will be transferred in lead-free configuration only, products in lead-present configuration will be converted as well according to PCN APG-AED/10/5437 dated April 1, 2010 (Passive Pad Implementation) already communicated. See enclosed reference table of new part numbers.
Change Product Identification	Letter code "G" on plant code traceability
Manufacturing Location(s)	1]Sc Carsem M - Malaysia

Table 3. List of Attachments

Customer Part numbers list	
Qualification Plan results	



Customer Acknowledgement of Receipt	**PCN APG-BAD/12/7432**
Please sign and return to STMicroelectronics Sales Office	**Dated 10 Sep 2012**
☐ Qualification Plan Denied	Name:
☐ Qualification Plan Approved	Title:
	Company:
☐ Change Denied	Date:
☐ Change Approved	Signature:

Remark

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DOCUMENT APPROVAL

Name	Function
Liporace, Nicola	Marketing Manager
Nicoloso, Riccardo	Product Manager
Minerva, Francesco	Q.A. Manager

Product Change Notification

VIPower M03/M03.5 in SOT-223: Transfer from assembly plant Carsem to Assembly plant Fujitsu.

INVOLVED P&L FAMILY: 30

WHAT:
Assembly of VIPower M03/M03.5 products housed in SOT-223 will be transferred from subcontractor Carsem (Malaysia) to Fujitsu (China).

WHY:
Logistic.

WHO:
All the Customers using below list of products.
Due to all the products will be transferred in lead-free configuration only, products in lead-present configuration will be converted as well according to PCN APG-AED/10/5437 (Passive pad implementation) dated April 1, 2010 already communicated.
Below the reference new part numbers.

CARSEM			FUJITSU		
Silicon Line	Current Part Number		Silicon Line	New Part Number	Notes
VN73*	09399028-E	->	VNL6	VNN1NV04PTR-E	Passive pad silicon versions according to PCN 5437 issued in April 2010
VN73*	9399028	->	VNL6	VNN1NV04PTR-E	
VN73*	VNN1NV0413TR	->	VNL6	VNN1NV04PTR-E	
VN79*	28006923	->	VNS2	VNN7NV04PTR-E	
VN79*	VNN7NV0413TR	->	VNS2	VNN7NV04PTR-E	
VN84*	VNN3NV0413TR	->	VNS6	VNN3NV04PTR-E	
VNL6	VNN1NV04PTR-E	->	VNL6	VNN1NV04PTR-E	
VNS2	VNN7NV04PTR-E	->	VNS2	VNN7NV04PTR-E	
VNS6	VNN3NV04PTR-E	->	VNS6	VNN3NV04PTR-E	

*No Passive Pad Silicon Version

WHEN:
Tentative date of change is: December 2012
Qualification report included to this PCN (RR002612CT2235).

WHERE:
Carsem (Malaysia) sending plant – Fujitsu (China) receiving plant.

SOT223 assembly process qualification in NANTONG FUJITSU subcontractor

General Informations	
Commercial Product	**VNN7NV04P-E**
Product Line	VNS2
Silicon process technology	VIPower M0_3.5
Package	SOT223

Locations	
Diffusion fab location	ST AMK6 Ang Mo Kio (Singapore)
Assembly plant location	Subcon Nantong Fujitsu (China)
Test plant location	ST Shenzhen (China)
Reliability lab location	ST Catania (Italy)

General Informations	
Commercial Product	**VNN3NV04P-E**
Product Line	VNS6
Silicon process technology	VIPower M0_3.5
Package	SOT223

Locations	
Diffusion fab location	ST CT6 Catania (Italy)
Assembly plant location	Subcon Nantong Fujitsu (China)
Test plant location	ST Shenzhen (China)
Reliability lab location	ST Catania (Italy)

General Informations	
Commercial Product	**VNN1NV04P-E**
Product Line	VNL6
Silicon process technology	VIPower M0_3.5
Package	SOT223

Locations	
Diffusion fab location	ST CT6 Catania (Italy)
Assembly plant location	Subcon Nantong Fujitsu (China)
Test plant location	ST Shenzhen (China)
Reliability lab location	ST Catania (Italy)

Author:
F. CERAULO
Product Qualification Eng
APG Q&R Catania

Reliability and electrical test executed by:
G. Foti
Rel. Eng.
IMS Rel Dept. – APG Support

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- 1. Reliability evaluations overview

1.1 Objectives

Aim of this report is to present the results of the reliability evaluations performed to qualify the subcontractor NANTONG FUJITSU (China) as new location to assembly in package **SOT223** the VIPower products designed in M0_3.5 technology.

The products chosen as test vehicles are: **VNN7NV04P-E** (VNS2 as ST internal code) and the **VNN1NV04P-E** (VNL6 as ST internal code) diffused in ST AMK6 Ang Mo Kio (Singapore), the **VNN3NV04P-E** (VNS6 as ST internal code) diffused in ST CT6 Catania (Italy).

The qualification was based on 3 lots, one lot per vehicle, according to the **AEC_Q100 Rev.G** specification the following tests were performed: Preconditioning (PC), Temperature Humidity Bias (THB), Autoclave (AC), Thermal Cycling (TC), Power Temperature Cycling (PTC), High Temperature Storage (HTS) as Accelerated Environment Stress (test Group A); High Temperature Operative Life (HTOL) as Accelerated Lifetime Simulation (test Group B); Wire Bond Pull/Shear tests (WBP, WBS), Solderability (SD), Physical Dimension (PD) as Package Assembly Integrity (test Group C); Gate Leakage (GL) as Electrical Verification (test Group E).

1.2 Results

All reliability tests have been completed with positive results, neither functional nor parametric rejects were detected at final electrical testing.

Based on the overall positive results we consider the products qualified from a reliability point of view.

- 2. Traceability

VNN7NV04P-E (VNS2)

Wafer fab information	
Wafer fab manufacturing location	ST AMK6 Ang Mo Kio (Singapore)
Wafer diameter (inches)	6
Silicon process technology	VIPower M0_3.5
Die finishing back side	Ti-Ni-Au
Die size (micron)	2540 x 2130
Metal levels / materials	1 level / AlSi (3.2 µm)
Die finishing front side	SiN/POLYIMIDE
Diffusion Lots #	6110J4T

Assembly Information	
Assembly plant location	SC - NANTONG FUJITSU (China)
Package description	SOT-223
Molding compound	SUMITOMO EMEG600F
Wires bonding materials/diameters	Au 2.0mils
Die attach material	SOFT SOLDER DIE ATTACH 95.5Pb/2Sn/2.5Ag
Assembly Lots #	Lot1: GK22012101

Final Testing Information	
Electrical testing manufacturing location	ST Shenzhen (China)

VNN3NV04P-E (VNS6)

Wafer fab information	
Wafer fab manufacturing location	ST CT6 Catania (Italy)
Wafer diameter (inches)	6
Silicon process technology	VIPower M0_3.5
Die finishing back side	Ti-Ni-Au
Die size (micron)	2540 x 2130
Metal levels / materials	1 level / AlSi (3.2 µm)
Die finishing front side	SiN/POLYIMIDE
Diffusion Lots #	3204134

Assembly Information	
Assembly plant location	SC - NANTONG FUJITSU (China)
Package description	SOT-223
Molding compound	SUMITOMO EMEG600F
Wires bonding materials/diameters	Au 2.0mils
Die attach material	SOFT SOLDER DIE ATTACH 95.5Pb/2Sn/2.5Ag
Assembly Lots #	Lot1: GK21917V01

Final Testing Information	
Electrical testing manufacturing location	ST Shenzhen (China)

VNN1NV04P-E (VNL6)

Wafer fab information	
Wafer fab manufacturing location	ST AMK6 Ang Mo Kio (Singapore)
Wafer diameter (inches)	6
Silicon process technology	VIPower M0_3.5
Die finishing back side	Ti-Ni-Au
Die size (micron)	1710 x 1520
Metal levels / materials	1 level / AlSi (3.2 µm)
Die finishing front side	SiN/POLYIMIDE
Diffusion Lots #	6811LPK

Assembly Information	
Assembly plant location	SC - NANTONG FUJITSU (China)
Package description	SOT-223
Molding compound	SUMITOMO EMEG600F
Wires bonding materials/diameters	Au 2.0mils
Die attach material	SOFT SOLDER DIE ATTACH 95.5Pb/2Sn/2.5Ag
Assembly Lots #	Lot1: GK8381VX01

Final Testing Information	
Electrical testing manufacturing location	ST Shenzhen (China)

- 3. VNN7NV04P-E - Devices characteristics

3.1 Generalities

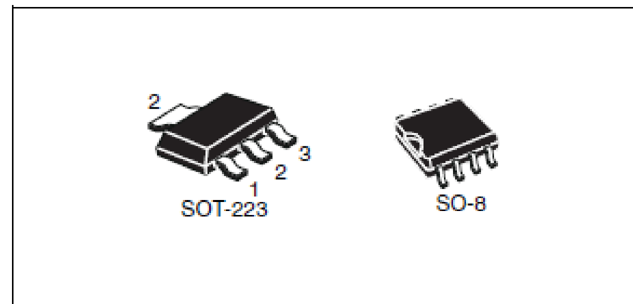
VNN7NV04P-E, VNS7NV04P-E

OMNIFET II
fully autoprotected Power MOSFET

Features

Type	$R_{DS(on)}$	I_{lim}	V_{clamp}
VNN7NV04P-E VNS7NV04P-E	60 mΩ	6 A	40 V

- Linear current limitation
- Thermal shutdown
- Short circuit protection
- Integrated clamp
- Low current drawn from input pin
- Diagnostic feedback through input pin
- ESD protection
- Direct access to the gate of the Power MOSFET (analog driving)
- Compatible with standard Power MOSFET in compliance with the 2002/95/EC European Directive

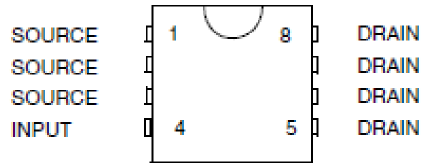


Description

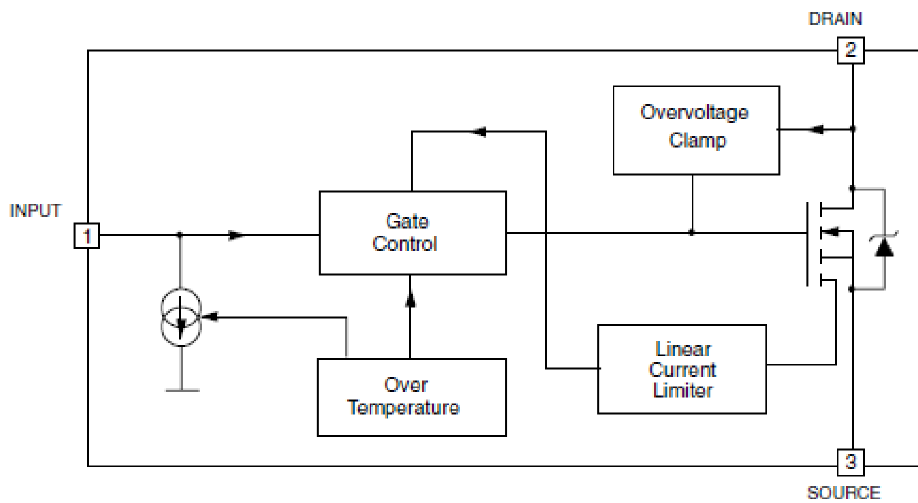
The VNN7NV04P-E, VNS7NV04P-E, are monolithic devices designed in STMicroelectronics VIPower™ M0-3 Technology, intended for replacement of standard Power MOSFETs from DC up to 50 kHz applications. Built in thermal shutdown, linear current limitation and overvoltage clamp protect the chip in harsh environments.

Fault feedback can be detected by monitoring the voltage at the input pin.

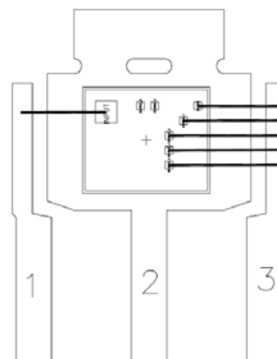
3.2 Pins connection



3.3 Blocks diagram



3.4 Bonding diagram



- 4. VNN3NV04P-E - Devices characteristics

4.1 Generalities

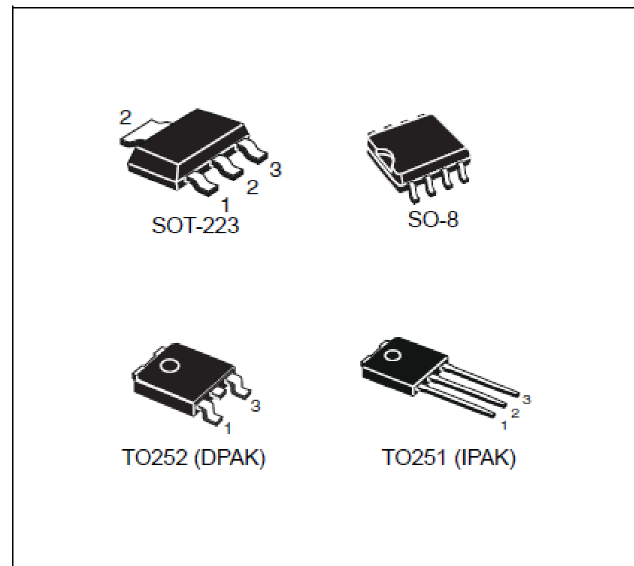
VNN3NV04, VNS3NV04 VND3NV04, VND3NV04-1

OMNIFET II
fully autoprotected Power MOSFET

Features

Type	$R_{DS(on)}$	I_{lim}	V_{clamp}
VNN3NV04 VNS3NV04 VND3NV04 VND3NV04-1	120 mΩ	3.5 A	40 V

- Linear current limitation
- Thermal shutdown
- Short circuit protection
- Integrated clamp
- Low current drawn from input pin
- Diagnostic feedback through input pin
- ESD protection
- Direct access to the gate of the Power MOSFET (analog driving)
- Compatible with standard Power MOSFET in compliance with the 2002/95/EC European Directive

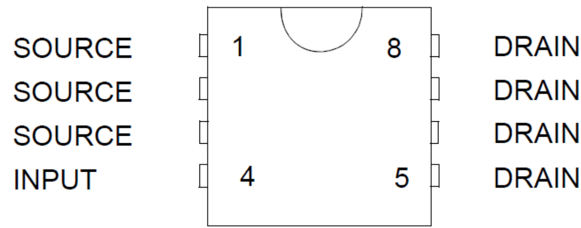


Description

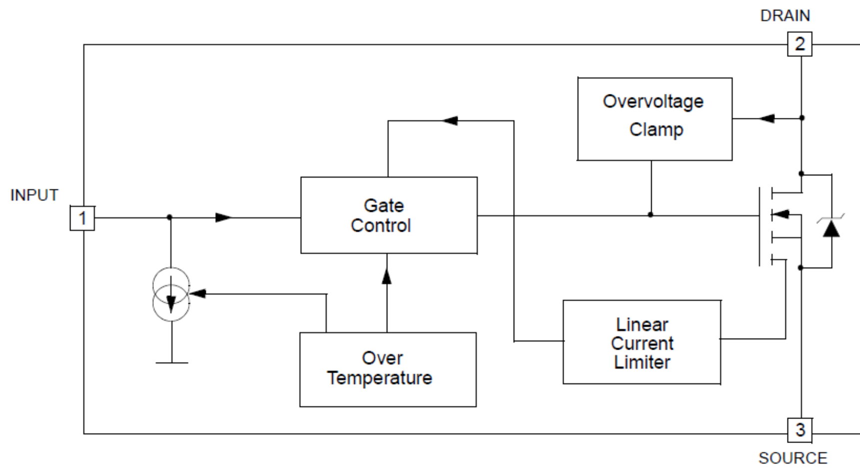
The VNN3NV04, VNS3NV04, VND3NV04 VND3NV04-1, are monolithic devices designed in STMicroelectronics™ VIPower™ M0-3 Technology, intended for replacement of standard Power MOSFETs from DC up to 50 kHz applications. Built in thermal shutdown, linear current limitation and overvoltage clamp protect the chip in harsh environments.

Fault feedback can be detected by monitoring the voltage at the input pin.

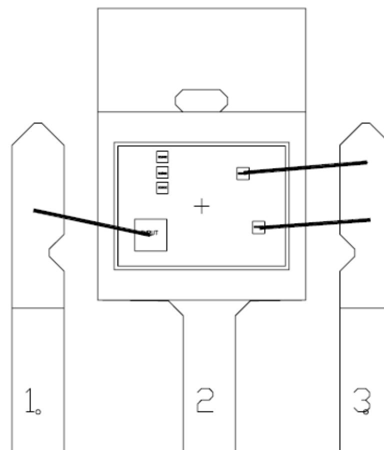
4.2 Pins connection



4.3 Blocks diagram



4.4 Bonding diagram



- 5. VNN1NV04P-E - Devices characteristics

5.1 Generalities

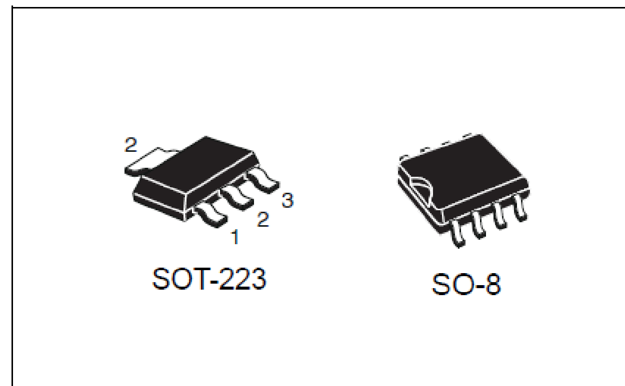
VNN1NV04P-E, VNS1NV04P-E

OMNIFET II
fully autoprotected Power MOSFET

Features

Parameter	Symbol	Value
Max on-state resistance (per ch.)	R_{ON}	250 mΩ
Current limitation (typ)	I_{LIMH}	1.7 A
Drain-source clamp voltage	V_{CLAMP}	40 V

- Linear current limitation
- Thermal shutdown
- Short circuit protection
- Integrated clamp
- Low current drawn from input pin
- Diagnostic feedback through input pin
- ESD protection
- Direct access to the gate of the Power MOSFET (analog driving)
- Compatible with standard Power MOSFET

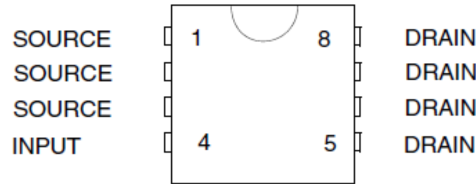


Description

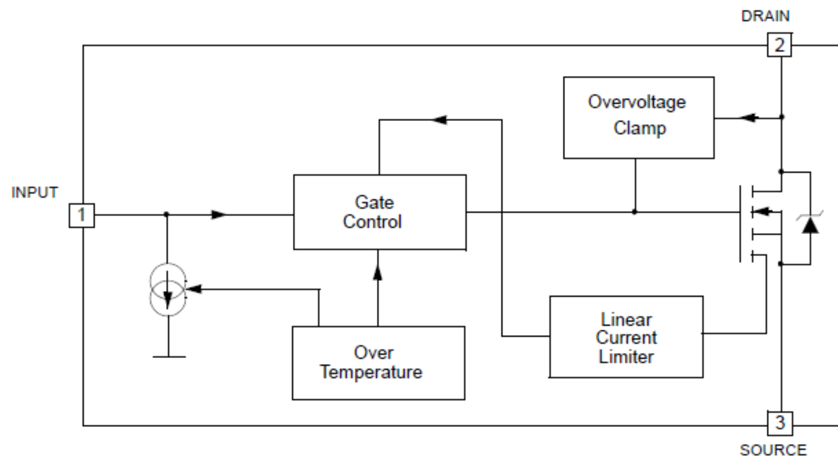
The VNN1NV04P-E, VNS1NV04P-E are monolithic devices designed in STMicroelectronics VIPower M0-3 Technology, intended for replacement of standard Power MOSFETs from DC up to 50 kHz applications. Built in thermal shutdown, linear current limitation and overvoltage clamp protect the chip in harsh environments.

Fault feedback can be detected by monitoring the voltage at the input pin.

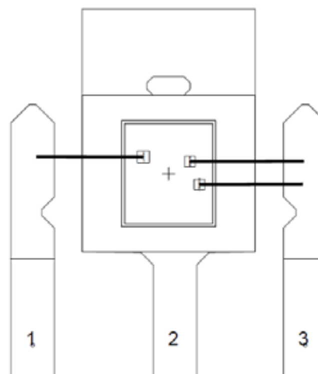
5.2 Pins connection



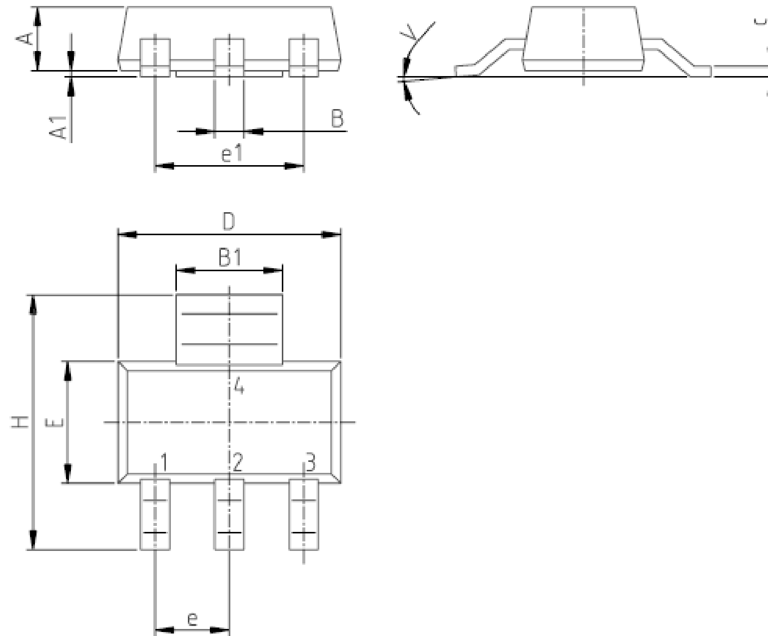
5.3 Blocks diagram



5.4 Bonding diagram



5.5 Package outline/Mechanical data



Dim.	mm.			inch		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.8			0.071
B	0.6	0.7	0.85	0.024	0.027	0.033
B1	2.9	3	3.15	0.114	0.118	0.124
c	0.24	0.26	0.35	0.009	0.01	0.014
D	6.3	6.5	6.7	0.248	0.256	0.264
e		2.3			0.09	
e1		4.6			0.181	
E	3.3	3.5	3.7	0.13	0.138	0.146
H	6.7	7	7.3	0.264	0.276	0.287
V	10° (max)					
A1	0.02		0.1	0.0008		0.004

- 6. Reliability qualification plan and results

AEC #	Test Name	STM Test Conditions	Sample Size/ Lots	Results Fails/SS/Lots	Comments
A1	**PC** Pre Cond	- Preconditioning according to level 3 Jedec JESD22-A113F - Reflow according to Jedec JSTD020D-1	Before THB, AC, TC, PTC, HTOL. Reliability executed on units soldered on PCB		
A2	**THB** Temp Humidity Bias	Ta=85ºC, RH=85%, Vcc=24V for 1000 hours	77/3	0/77/3	
A3	**AC** Autoclave	Ta=121ºC, Pa=2atm, RH=100% for 96 hours	77/3	0/77/3	
A4	**TC** Temp. Cycling	Ta=-65ºC / +150ºC for 500 cycles	77/3	0/77/3	
A5	**PTC** Power Temp. Cycling	Per JA105. Ta=-40ºC / +125ºC for 1000 cycles. Test before and after at room and hot temperatures.	45/1	0/45/1	
A6	**HTSL** High Temp. Storage Life	Ta=150ºC for 1000 hours. TST before and after at room and hot temperatures.	45/3	0/45/3	
B1	**HTOL** High Temp. Op. Life	Bias Static stress (JESD22-A108): Ta=**150ºC**, Vcc=32V for **1000 hours**	77/3	0/77/3	
C1	**WBS** Wire Bond Shear	Per AEC-Q100-001. See Appendix 3 procedure. 0 and Ppk >= 1.66 or Cpk >= 1.33	30 bonds from minimum 5 of units	Passed	
C2	**WBP** Wire Bond Pull	Per MIL-STD883, M2011 Condition C or D. 0 and Ppk >= 1.66 or Cpk >= 1.33	30 bonds from minimum 5 of units	Passed	
C3	**SD** Solderability		15/1	Passed	
C4	**PD** Physical Dimensions		10/3	Passed	
E8	**GL** Gate Leakage		6/1	Passed	

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